forming a semiconductor layer on the semiconductor substrate;

forming first trenches in a surface of the semiconductor layer;

heating the semiconductor layer having the first trenches in a non-oxidizing and non-nitridizing atmosphere containing a dopant or a compound that includes the dopant in order to smooth surfaces defining the first trenches and to diffuse the dopant contained in the non-oxidizing and non-nitridizing atmosphere into the semiconductor layer and partially increase a dopant concentration in the semiconductor layer to form one layer out of a first conductivity type drift layer and a second conductivity type layer on the semiconductor substrate that have a predetermined dopant concentration;

forming the other layer out of the first conductivity type drift layer and the second conductivity type layer to fill the first trenches by epitaxial growth in order to form an alternate arrangement of first conductivity type drift regions and second conductivity type first semiconductor regions;

forming first conductivity type second semiconductor regions on the first conductivity type drift regions;

forming a second conductivity type base layer on the first semiconductor regions and the second semiconductor regions;

forming second trenches that extend through the base layer to reach the second semiconductor regions;

forming gate insulating films on surfaces defining the second trenches; and

forming gate electrodes on the gate insulating films.

6. The method according to claim 5, wherein the semiconductor layer is formed to have a dopant concentration lower than that in the one layer out of the doped first conductivity type drift layer and the doped second conductivity type layer and wherein the semiconductor layer is heated such that the one layer is formed at an area except for outermost ends of the semiconductor layer and a low dopant concentration region is formed to be adjacently located outside the one layer at the outermost ends.

7. The method according to claim 4, wherein a dopant concentration in the predetermined layer is within the range of 1×10^{15} to 1×10^{18} cm^{-3} and a dopant concentration in the one layer is within the range of 1×10^{14} to 1×10^{19} cm^{-3}.

8. The method according to claim 4, wherein the dopant contained in the non-oxidizing and non-nitridizing atmosphere has the same conductivity type as that of the predetermined layer.

9. The method according to claim 1, wherein the non-oxidizing and non-nitridizing atmosphere includes hydrogen or a rare gas.

10. The method according to claim 1, wherein the non-oxidizing and non-nitridizing atmosphere has a pressure lower than that of the atmospheric pressure.

11. The method according to claim 1, wherein the dopant contained in the non-oxidizing and non-nitridizing atmosphere is one element selected from the group consisting of boron (B), phosphorus (P), arsenic (As), and antimony (Sb).

12. The method according to claim 1, wherein the semiconductor layer is heated at a temperature in the range of 1000 to 1150° C.

13. The method according to claim 4, wherein the non-oxidizing and non-nitridizing atmosphere includes hydrogen or a rare gas.

14. The method according to claim 4, wherein the non-oxidizing and non-nitridizing atmosphere has a pressure lower than that of the atmospheric pressure.

15. The method according to claim 4, wherein the dopant contained in the non-oxidizing and non-nitridizing atmosphere is one element selected from the group consisting of boron (B), phosphorus (P), arsenic (As), and antimony (Sb).

16. The method according to claim 4, wherein the semiconductor layer is heated at a temperature in the range of 1000 to 1150° C.

17. A semiconductor device comprising:

a first conductivity type semiconductor substrate, which forms a drain region;

first conductivity type drift regions;

second conductivity type first semiconductor regions, wherein the drift regions and the first semiconductor regions are in alternate contact with each other-to laterally form an alternately arranged area;

first conductivity type second semiconductor regions, which are located on the drift regions;

second conductivity type base regions, which are located on the first semiconductor regions and the second semiconductor regions;

second trenches, which extend through the base regions to reach the second semiconductor regions;

gate insulating films, which are located on surfaces of the second trenches;

forming gate electrodes, which are located on the gate insulating films; and

a low dopant concentration region, which is adjacently located outside the alternately arranged area, which is made of the drift regions and the first semiconductor regions, wherein the low dopant concentration region has a dopant concentration lower than those of the drift regions and the first semiconductor regions.

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